

Code: EE5T6

**III B.Tech - I Semester – Regular/ Supplementary Examinations  
October 2017**

**LINEAR AND DIGITAL INTEGRATED CIRCUIT  
APPLICATIONS  
(ELECTRICAL & ELECTRONICS ENGINEERING)**

Duration: 3 hours

Max. Marks: 70

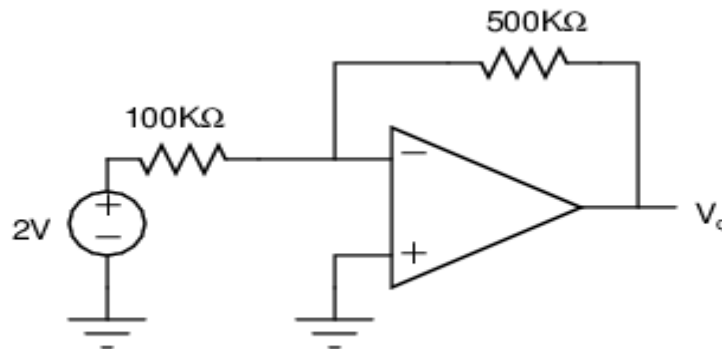
**PART – A**

Answer *all* the questions. All questions carry equal marks

11 x 2 = 22 M

1.

- a) In op-amp specifications, define slew-rate and how it is calculated?
- b) Calculate the output voltage  $V_o$ .



- c) What are the two requirements for generation of oscillations in oscillator circuits?
- d) How filters are classified into first order and second order?

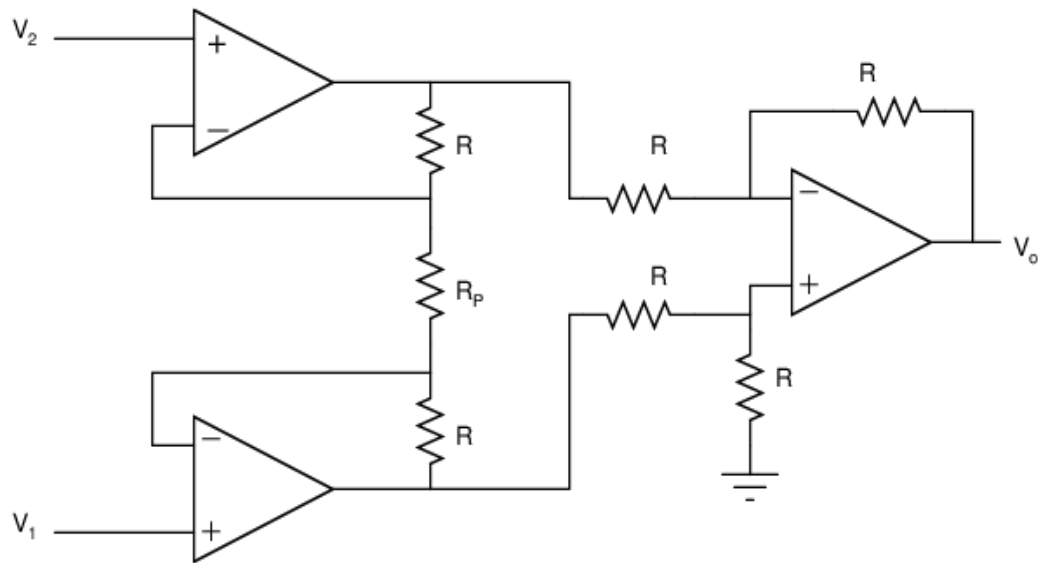
- e) Draw a simple block diagram of a voltage controlled oscillator.
- f) Define capture range of a PLL circuit.
- g) Write down any two applications of multiplexer and decoder.
- h) Draw the block diagram of a 2bit Ripple Carry look ahead adder.
- i) Write down the characteristic table of a JK Flipflop.
- j) Draw the block diagram of a mod-2 counter.
- k) What is meant by 3dB cutoff frequency in filters?

## PART – B

Answer any *THREE* questions. All questions carry equal marks.

3 x 16 = 48 M

- 2.a) Write down the differences between a practical op-amp and an ideal op-amp. 8 M
  
- b) Derive the expression for  $V_o$  interms of  $V_1$  &  $V_2$  for the instrumentation amplifier given below. 8 M



3.a) Draw the diagram of a Wien bridge oscillator and explain its operation. 8 M

b) Realize/design a passive element (resistor) using switch capacitor filters technique, explain its working principle. Write down few advantages of switch capacitor filters. 8 M

4.a) Draw the block diagram of a PLL circuit. Explain the operation of each block. 8 M

b) Give an example of a digital phase detector used in PLL circuit. 8 M

5.a) Design a combinational multiplier over A(3bits) and B(2bits). 8 M

b) Realize a full adder with

i) 2x1 multiplexer and

ii) Half adders.

8 M

6.a) Design a mod-10 counter using Johnson counter and write down its operation and mention generated state sequence.

10 M

b) With the help of block diagram, explain the working principle of a Serial in parallel out shift register.

6 M